3 DSP/Analog Hardware Reference

Overview

[@j DSP/Analog Hardware Reference Overview]

DSP/Analog Hardware Reference is a collection of information which may be helpful when creating user-defined C/C++, MATLAB, or Visual Basic applications need to work with supported DSP/analog hardware.

This chapter section is *programming-oriented, and not operation-oriented.* It is not intended to provide information about individual hardware types. For detailed information about specific DSP/analog hardware types, see section 3.1 below, DSP/Analog Hardware Documentation.

Main Topics

DSP/Analog Hardware Documentation

Board Designator, Driver ID, and Classification Table

3.1 DSP/Analog Hardware Documentation

As mentioned in the DSP/Analog Hardware Reference Overview section above, information in this chapter section is not intended to speak to individual DSP/analog hardware types. Here is a list of places to look for additional DSP/analog hardware information:

Hypersignal-Macro Series Hardware Reference Guide (most complete source by far)

Signalogic DSP Software Users Guide chapter 4, Using DSP Source Code Interface Software

section 3.2 below, Board Designator, Driver ID, and Classification Table

section 3.3 below, Hypersignal DSP Source Code Variable List

Signalogic DSP Software System Guide section 4.3, Troubleshooting DSP/Analog Hardware Problems

Signalogic DSP Software System Guide section 4.3.1, I/O-Mapped Hardware Conflicts

Signalogic DSP Software System Guide section 4.3.2, Memory-Mapped Transfer Gotchas

Signalogic DSP Software System Guide section 4.3.3, Host PC Internal Bus Speed Conflicts

Signalogic DSP Software System Guide section 4.3.4, Data Acquisition Problems

Signalogic DSP Software Users Guide section 4.3, DSPower-HWLib Function Overview

Signalogic DSP Software Users Guide section 4.5, Acquiring Data Using DSPower-HWLib Software

Signalogic DSP Software Users Guide section 8.2, Hardware Selector

Signalogic DSP Software Users Guide section 8.3, Hardware Setup File

DSP/Analog Hardware Solutions Guide (marketing brochure which contains partial summary of DSP/analog hardware types)

3.2 Board Designator, Driver ID, and Classification Table

Listed below are current valid Board Designators which can be used in the DSAssignBoard, DSGetHWMgrCurVal, DSSetHWMgrCurVal, DSShowHardwareSelectorDlg, and DSGetHWMgrEntryIndex calls in Hardware Library and Hardware Manager (DSPower-HWLib software).

Values corresponding to Board Designators which are also shown include description, manufacturer, Driver IDs, DSP code classification and subclassification, and default DSP Program File. The table below is organized alphabetically by manufacturer (as is the Hardware Selector in Hardware Manager), to hopefully make finding Board Designators easier.

Manufacturer	Board Designator	Description	Driver IDs	CIs	Default DSP Program File
Ariel	ARI320	DSP-16	2,0	1,0	tms32025.out
Ariel	ARI32C	DSP-32C	30,0	1,0	dsp32c.out
Ariel	ARI56	DSP-56	29,4	5,0	dsp56000.out
Ariel	ARI96	DSP-96	80,0	1,0	dsp96000.out
Ariel	ARI3210	MP3210	85,0	0,0	dsp3210.out
Ariel	ARI3210/1	MP3210 (second processor)	85,0	0,0	dsp3210.out
Ariel	ARIC40	DSP-C40	45,0	0,0	tms32040.out
Ariel	ARIC40-B	DSP-C40U (SRAM only)	45,4	0,0	tms32040.out
Ariel	ARI320-B	PC-C25	2,4	1,1	tms32025.out
Ariel	ARI56-B	PC-56	29,0	2,0	dsp56000.out
Ariel	ARI56-B	PC-56D with onboard I/O	29,0	2,0	dsp56000.out
Ariel	ARI56-D	DatPort with PC-56D	29,6	6,0	dsp56000.out
Ariel	ARI56-D	ProPort with PC-56D	29,6	6,0	dsp56000.out
Ariel	ARI56-DX	ProPort w/ PC-	29,6	6,0	dsp56000.out

		56D, 100 kHz			
Ariel	ARI3210-B	ProPort w/ MP3210	85,0	0,0	dsp3210.out
Ariel	ARI56-DM	Dig. Microphone with PC-56D	29,38	6,0	dsp56000.out
Ariel	ARI32C-B	ProPort with PC-32C	30,4	1,1	dsp32c.out
Ariel	ARI32C-B	DatPort with PC-32C	30,4	1,1	dsp32c.out
AT&T	ATT32C	DSP32C development board	31,0	2,0	dsp32c.out
ASPI	ASPIC30	Banshee (TMS-320C30)	59,0	1,0	tms32030.out
ASPI	ASPIC30-AD16	Banshee with AD16 daughterbd	59,0	1,0	tms32030.out
CAC	CAC32	DSP32-PC	10,0	0,0	dsp32.out
CAC	CAC32C	DSP32C-AT	32,0	3,0	dsp32c.bin
CAC	CAC32C-COD	AC5 with CODEC daughterbd	32,6	3,3	dsp32c.out
CAC	CAC32C-DBD	AC5 with DBDADA daughterbd	32,5	3,2	dsp32c.out
CAC	CAC32C-DBC	AC5 with DBCS5339 daughterbd	32,4	3,1	dsp32c.out
CAC	CAC3210	QUANTUMdsp DSP3210	86,0	1,0	dsp3210.out
Data Translation	DT2821	DT2821 series	70,0	N/A	N/A
Data Translation	DT2823	DT2823 series	70,0	N/A	N/A
Digital Audio Labs	DRB1	Digital Recording Board I	72,0	N/A	N/A
Digital Audio Labs	DRB2	Digital Recording Board II	72,0	N/A	N/A
DSP Research	DRIC30	TIGER 30	53,0	4,0	tms32030.out
DSP Research	DRIC30-BB71	TIGER 30 with BB71 (rev. B)	53,5	4,2	tms32030.out
Domain Technologies	DOMC31	DSPCard-C31	56,0	3,0	tms32030.out
Electronic Tools	ET56	miniKit 56001	23,0	9,0	dsp56000.out
Innovative	IIC31	PC31	55,0	6,0	tms32030.out

Integration					
Innovative Integration	IIC31-B	PC31, no dual-port SRAM	55,4	6,0	tms32030.out
Innovative Integration	IIC50	PC50	5,0	0,0	tms32050.out
Innovative Integration	IIC50-B	PC50, no dual-port SRAM	5,4	0,0	tms32050.out
Intelligent Instrumentation	PCI41C	PCI20041C (auto config)	60,0	N/A	N/A
Intelligent Instrumentation	PCI202C	PCI20202C (auto config)	9,0	3,0	tms32025.out
Intelligent Instrumentation	ZPB32-ZPB100	ZPB32 (DSP32) with ZPB100	14,0	1,0	dsp32.bin
Intelligent Instrumentation	ZPB32-ZPD1002	ZPB32 (DSP32) with ZPD1002	14,0	1,0	dsp32.bin
Intelligent Instrumentation	ZPB32-ZPD1007	ZPB32 (DSP32) with ZPD1007	14,0	1,0	dsp32.bin
Intelligent Instrumentation	ZPB32-ZPB1100	ZPB32 (DSP32) with ZPB1100	14,4	1,0	dsp32.bin
Intelligent Instrumentation	ZPB32-ZPB2100	ZPB32 (DSP32) with ZPB2100	14,4	1,0	dsp32.bin
Intelligent Instrumentation	ZPB34-ZPB100	ZPB34A (DSP32C) with ZPB100	33,6	4,3	dsp32c.out
Intelligent Instrumentation	ZPB34-ZPD1002	ZPB34A (DSP32C) with ZPD1002	33,0	4,0	dsp32c.out
Intelligent Instrumentation	ZPB34-ZPD1007	ZPB34A (DSP32C) with ZPD1007	33,3	4,0	dsp32c.out
Intelligent Instrumentation	ZPB34-ZPB1100	ZPB34A (DSP32C) with ZPD1100	33,4	4,2	dsp32c.out
Intelligent Instrumentation	ZPB34-ZPB2100	ZPB34A (DSP32C) with ZPD2100	33,4	4,2	dsp32c.out
Intelligent Instrumentation	ZPB34-ZPB6064	ZPB34A (DSP32C) with ZPB6064	33,5	4,1	dsp32c.out
Loughborough Sound Images	LSI320	TMS320C25 system board	0,0	0,0	tms32025.out
Loughborough Sound Images	LSI56	DSP56001 system board	20,0	0,0	dsp56000.out

Loughborough Sound Images	LSI32C	DSP32C system board	39,0	0,0	dsp32c.out
Loughborough Sound Images	LSIC30	TMS320C30 system board	50,0	0,0	tms32030.out
Loughborough Sound Images	LSI2101	ADSP-2101 system board	44,0	0,0	adsp21x.exe
Loughborough Sound Images	LSI96	DSP96002 system board	84,0	0,0	dsp96000.out
Motorola	ADS56-A	ADS dev sys with Ariel ADC56000	21,0	1,0	dsp56000.out
Motorola	ADS56-B	ADS dev sys with ADC16 eval I/O	21,4	4,0	dsp56000.out
MTT Instrumentation	MTT32C	Lory DSP4100	34,0	5,0	dsp32c.out
MTT Instrumentation	MTTC30	Lory DSP4200	54,0	5,0	tms32030.out
National Instruments	NAT32C	AT-DSP2200	35,0	6,0	dsp32c.out
Peralex	PA56	PROTO-56	29,5	2,0	dsp56000.out
Quantawave	QWV32C	Qw32C-8AFA	36,0	7,0	dsp32c.out
Signalogic	SIG32C	Sig32C-8	36,0	7,0	dsp32c.out
Sonitech	SONC30	Spirit-30	51,0	2,0	tms32030.out
Sonitech	SONC30-SAIB	Spirit-30 with SAIB	51,4	2,1	tms32030.out
Sonitech	SONC30-STIB	Spirit-30 with STIB	51,4	2,1	tms32030.out
Techron	TEF20HI	TEF20HI with direct mic input	21,6	8,0	dsp56000.out
Texas Instruments	SWDS	SWDS (TMS-320C25)	1,0	2,0	tms32025.out
Texas Instruments	SWDS-AIB	SWDS with AIB-2 input board	1,0	2,0	tms32025.out
Texas Instruments	EVMC30	EVM (TMS-320C30)	52,0	3,0	tms32030.out
Turtle Beach Systems	TBS56	MultiSound	22,0	3,0	dsp56tbs.out
Turtle Beach Systems	TBS56-B	Tahiti	22,4	3,0	dsp56tbs.out

Notes

1) **Cls** in the table heading above is an abbreviation for **classification**. Classification values above are shown as "main,sub" values. The "main" value can be used with the DSP_BOARDCLASS DSP source code variable, and the "sub" value with the DSP_BOARDSUBCLASS variable. Note that the DSGetBoardClass call in Hardware Library returns a WORD value as follows:

DSGetBoardClass =>> main*256 + sub

2) N/A (not applicable) as used above means the hardware type does not have a DSP device.

3) Driver ID values above are shown "major,minor" values. Note that the DSGetBoardInfo call with DS_GBI_DRIVERID parameter returns a Driver ID value in the form:

wDriverID = minor*256 + major

For more information see Driver ID Fields in Hardware Setup File, in Signalogic DSP Software Users Guide section 8.3.1, Hardware Setup File Fields.

4) Note that in some cases similar DSP/analog hardware types look identical to host computer (Driver ID values are same), but different from the onboard DSP device's point of view. This typically occurs when the same manufacturer builds boards with differ only with analog I/O capabilities. On the other hand, some DSP/analog hardware types look the same from to the onboard DSP, but different from the host's point of view. This usually occurs when different manufacturers build boards which have similar DSP, memory, and analog I/O characteristics.

3.3 Hypersignal DSP Source Code Variable List

Listed below are pre-defined constants which can be used in DSGetHVarMem and DSPutHVarMem calls in Hardware Library (DSPower-HWLib software), in order to control and communicate with DSP code executing in conjunction with Hypersignal acquisition, generation, instrument, and file-based acceleration functions. These calls, as well as the DSGetMem and DSPutMem calls, can be invoked either while the DSP is executing or in a static state.

Related Documentation TopicsSections

Signalogic DSP Software Users Guide section 5.0.2, DSP Source Code Interfaces for Hypersignal

Signalogic DSP Software Users Guide section 5.0.3, DSP Source Code Interfaces for Hypersignal in Engine Mode

Hypersignal-Macro Series Hardware Reference Guide chapter 4, DSP Source Code Interface

Hypersignal-Macro Series Hardware Reference Guide Appendix A, WriteDSPVal Constants

See Also

DSGetHVarMem

DSPutHVarMem

Hypersignal DSP Source Code Variables

DSP_ADCOUNT

DSP_BOARDCLASS

DSP_BOARDSUBCLASS

DSP_BUFLEN

DSP_BUFNUM

DSP_BUSYFLG

DSP_CHANLIST

DSP_CODECCTRL1

DSP_CODECCTRL2

DSP_COUPLIST

DSP_DACOUNT

DSP_DUPFLG

DSP_FILTADDR1

DSP_FILTADDR2

DSP_FILTLEN1

DSP_FILTLEN2

DSP_FILTTYPE1

DSP_FILTTYPE2

DSP_FILTQUANT

DSP_FILTUPDFLG

DSP_FFTLEN

DSP_FFTORD

DSP_FRMSIZ

DSP_FSMODE

DSP_FSVALUE

DSP_GAINLIST

DSP_HOSTBUFNUM

DSP_IOMODULE

DSP_LOGCOEFFA

DSP_LOGCOEFFB

DSP_LOGFLG1

DSP_LOGFLG2

DSP_MAGDATAADDR

DSP_MAXVAL

DSP_MAXVAL1

DSP_MAXVAL2

DSP_MAXVALIMAG

DSP_MAXVALREAL

DSP_MINVAL

DSP_MONITORFLG

DSP_NUMCHAN

DSP_OFFSETIN

DSP_OFFSETOUT

DSP_OPMODE

DSP_OVERFLOW

DSP_PHZREQ

DSP_PWRCOEFFA

DSP_PWRCOEFFB

DSP_PWRFLG1

DSP_PWRFLG2

DSP_RIDATAADDR

DSP_RIFLG

DSP_SCALEIN

DSP_SCALEOUT

DSP_SERIALCTRL

DSP_STMBUFLEN

DSP_STMDATAADDR

DSP_TIMDATAADDR

DSP_TRIGCHANLIST

DSP_TRIGLEVEL

DSP_WINSCL

DSP_WINDATAADDR

DSP_XFERFLG1

DSP_XFERFLG2

DSP_ADCOUNT

Description

Acquisition delay counter, in samples.

See Also

DSP_DACOUNT

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_BOARDCLASS

Description

Board classification number used in DSP code.

Comments

DSP/analog hardware types are classified by number. If hardware types are close related, with only minor differences such as analog I/O characteristics, DSP_BOARDSUBCLASS may be used.

See Also

DSP_BOARDSUBCLASS

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_BOARDSUBCLASS

Description

Board subclassification number used in DSP code.

Comments

DSP/analog hardware types are normally classified by the DSP_BOARDCLASS variable. If hardware types are close related, with only minor differences such as analog I/O characteristics, DSP_BOARDSUBCLASS may be used.

See Also

DSP_BOARDCLASS

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_BUFLEN

Description

Buffer length used in acquisition, generation, instrument, or file-based acceleration processing functions.

See Also

DSP_FRMSIZ

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_BUFNUM

Description

Current DSP buffer flag in continuous analog I/O functions which use a buffer-switching mechanism.

See Also

DSP_HOSTBUFNUM

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_BUSYFLG

Description

DSP busy flag.

Comments

Used by file-based acceleration processing functions to indicate when function is busy or idle.

See Also

DSP_RIFLG

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_CHANLIST

Description

Analog input channel list.

Comments

Each trace occupies a 4-bit channel field in this value, starting with trace 0 in bits 0..3.. For DSP/analog hardware types with 32-bit floating-point DSP devices, this normally means a maximum of 8 channels can be specified.

See Also

DSP_COUPLIST

DSP_GAINLIST

DSP_TRIGCHANLIST

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_CODECCTRL1

Description

CODEC control word 1.

Comments

Used only by DSP/analog hardware types with analog I/O CODEC devices which have special configuration settings or options not controllable by standard DSP variables sent from the DSP Engine. Examples of non-standard settings include sin(x)/x filter enable/disable, µLaw vs. linear data format, bit-order reversal, etc.

See Also

DSP_CODECCTRL2

DSP_SERIALCTRL

DSP_FSMODE

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_CODECCTRL2

Description

CODEC control word 2.

Comments

Used only by DSP/analog hardware types with analog I/O CODEC devices which have special configuration settings or options not controllable by standard DSP variables sent from the DSP Engine. Examples of non-standard settings include sin(x)/x filter enable/disable, µLaw vs. linear data format, bit-order reversal, etc.

See Also

DSP_CODECCTRL1

DSP_SERIALCTRL

DSP_FSMODE

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_COUPLIST

Description

Analog input coupling list.

Comments

Each input trace occupies a 4-bit channel field in this value, starting with trace 0 in bits 0..3. Currently defined values include 0 = dc coupling, 1 = ac coupling, 2 = microphone input, 3 = auxiliary input. For DSP/analog hardware types with 32-bit floating-point DSP devices, this normally means a maximum of 8 channels can be specified.

See Also

DSP_CHANLIST

DSP_GAINLIST

DSP_TRIGCHANLIST

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_DACOUNT

Description

Stimulus output delay counter, in samples.

See Also

DSP_ADCOUNT

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_DUPFLG

Description

Duplicate trace flag.

Comments

Set if instrument function trace 2 should be duplicated from trace 1.

See Also

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_FILTADDR1

Description

Filter coefficient address for trace 1 in acquisition, generation, and instrumentation functions if real-time filtering is enabled.

Comments

Filter coefficients are either in floating-point or quantized fixed-point form, depending on the DSP device in use. Onchip DSP memory is used, if possible, for optimal real-time performance.

See Also

DSP_FILTLEN1

DSP_FILTTYPE1

DSP_FILTQUANT

DSP_FILTUPDFLG

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_FILTADDR2

Description

Filter coefficient address for trace 2 in acquisition, generation, and instrumentation functions if real-time filtering is enabled.

Comments

Filter coefficients are either in floating-point or quantized fixed-point form, depending on the DSP device in use. Onchip DSP memory is used, if possible, for optimal real-time performance.

See Also

DSP_FILTLEN2

DSP_FILTTYPE2

DSP_FILTQUANT

DSP_FILTUPDFLG

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_FILTLEN1

Description

Length of filter for trace 1 in acquisition, generation, and instrumentation functions if real-time filtering is enabled.

Comments

Specifies number of taps for FIR filter, filter order for IIR filters. A value of 0 indicates real-time filtering for trace 1 is disabled.

See Also

DSP_FILTADDR1

DSP_FILTLEN1

DSP_FILTQUANT

DSP_FILTUPDFLG

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_FILTLEN2

Description

Length of filter for trace 2 in acquisition, generation, and instrumentation functions if real-time filtering enabled.

Comments

Specifies number of taps for FIR filter, filter order for IIR filters. A value of zero indicates real-time filtering for trace 2 is disabled.

See Also

DSP_FILTADDR2

DSP_FILTTYPE2

DSP_FILTQUANT

DSP_FILTUPDFLG

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_FILTTYPE1

Description

Type of filter for trace 1 in acquisition, generation, and instrumentation functions if real-time filtering is enabled.

Comments

Specifies FIR filter, IIR filter modified direct form, or IIR filter balanced pole-zero form.

See Also

DSP_FILTADDR1

DSP_FILTLEN1

DSP_FILTQUANT

DSP_FILTUPDFLG

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_FILTTYPE2

Description

Type of filter for trace 2 in acquisition, generation, and instrumentation functions if real-time filtering is enabled.

Comments

Specifies FIR filter, IIR filter modified direct form, or IIR filter balanced pole-zero form. A value of −1 indicates that filter is identical to filter 1.

See Also

DSP_FILTADDR2

DSP_FILTLEN2

DSP_FILTQUANT

DSP_FILTUPDFLG

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_FILTQUANT

Description

Filter coefficient and delay storage element quantization, in bits, used in acquisition, generation, and instrumentation functions which allow real-time filtering

See Also

DSP_FILTADDR1

DSP_FILTLEN1

DSP_FILTTYPE1

DSP_FILTUPDFLG

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_FILTUPDFLG

Description

Filter coefficient update flag used in acquisition, generation, and instrumentation functions which allow real-time filtering.

Comments

Indicates that filter coefficients have changed and should be updated. Used mostly by DSP/analog hardware types which have onchip memory not accessible by the host, which requires filter coefficients to be moved into onchip memory from external memory when an update has occurred.

See Also

DSP_FILTADDR1

DSP_FILTLEN1

DSP_FILTTYPE1

DSP_FILTUPDFLG

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_FFTLEN

Description

FFT length used in FFT processing functions and spectrum analyzer function.

See Also

DSP_FFTORD

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_FFTORD

Description

FFT order used in FFT processing functions and spectrum analyzer function.

See Also

DSP_FFTLEN

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_FRMSIZ

Description

Framesize, in samples.

Comments

Used in file-based acceleration processing for DSP and math functions. Not used to control data acquisition, generation, or instrumentation buffer lengths.

See Also

DSP_BUFLEN

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_FSMODE

Description

Sampling rate clock generator mode or control register value.

Comments

Value used to initialize counter, timer, clock generator, etc. on DSP/analog hardware used to generate sampling frequency for analog I/O functions. This value is normally calculated by DSP Engine, which takes into account discrete value, timer wordlength, or other limitations of DSP/analog hardware.

See Also

DSP_FSVALUE

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_FSVALUE

Description

Actual sampling rate value, in Hz.

Comments

Actual sampling frequency value being used after DSP_FSMODE value has been determined. DSP_FSMODE is normally calculated by the DSP Engine, which takes into account discrete value, timer wordlength, or other limitations of DSP/analog hardware. Note that for DSP/analog hardware with 16-bit memory width, this value may not correctly reflect sampling rates greater than 65535.

See Also

DSP_FSMODE

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_GAINLIST

Description

Analog input gain list.

Comments

Each trace occupies a 4-bit channel field in this value, starting with trace 0 in bits 0..3.. For DSP/analog hardware types with 32-bit floating-point DSP devices, this normally means a maximum of 8 channels can be specified.

See Also

DSP_CHANLIST

DSP_COUPLIST

DSP_TRIGCHANLIST

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_HOSTBUFNUM

Description

Current host buffer flag in continuous analog I/O functions which use a buffer-switching mechanism.

See Also

DSP_BUFNUM

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_IOMODULE

Description

I/O module indicator.

Comments

Currently only used by limited number of TMS320C25 hardware types.

See Also

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_LOGCOEFFA

Description

Log magnitude scaling coefficient "a".

Comments

Used in spectrum analyzer function when log magnitude calculation is in effect. Applied in equation of form $Ylog(x) = a*log_{10}[Ylin(x)] + b$.

See Also

DSP_LOGCOEFFB

DSP_LOGFLG1

DSP_LOGFLG2

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_LOGCOEFFB

Description

Log magnitude scaling coefficient "b".

Comments

Used in spectrum analyzer function when log magnitude calculation is in effect. Applied in equation of form $Ylog(x) = a*log_{10}[Ylin(x)] + b$.

See Also

DSP_LOGCOEFFA

DSP_LOGFLG1

DSP_LOGFLG2

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_LOGFLG1

Description

Log magnitude calculation request flag for trace 1.

Comments

Used by spectrum analyzer function.

See Also

DSP_LOGFLG2

DSP_LOGCOEFFA

DSP_LOGCOEFFB

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_LOGFLG2

Description

Log magnitude calculation request flag for trace 2.

Comments

Used by spectrum analyzer function.

See Also

DSP_LOGFLG1

DSP_LOGCOEFFA

DSP_LOGCOEFFB

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_MAGDATAADDR

Description

Frequency domain or wavelet domain magnitude/phase data base address.

Comments

For DSP/analog hardware with linear memory, magnitude and phase values alternate locations. For hardware with vector memory, magnitude values are in X: memory and phase values in Y: memory.

See Also

DSP_RIDATAADDR

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_MAXVAL

Description

Maximum absolute value found in processing buffer.

See Also

DSP_MAXVALIMAG

DSP_MAXVALREAL

DSP_MINVAL

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_MAXVAL1

Description

Current maximum absolute amplitude value for trace 1 in data acquisition functions.

See Also

DSP_MAXVAL

DSP_MAXVAL2

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_MAXVAL2

Description

Current maximum absolute amplitude value for trace 2 in data acquisition function.

See Also

DSP_MAXVAL

DSP_MAXVAL1

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_MAXVALIMAG

Description

Maximum absolute value of imaginary component of complex data found in processing buffer.

See Also

DSP_MAXVAL

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_MAXVALREAL

Description

Maximum absolute value of real component of complex data found in processing buffer.

See Also

DSP_MAXVAL

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_MINVAL

Description

Minimum value found in acquisition or processing buffer.

See Also

DSP_MAXVAL

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_MONITORFLG

Description

Monitor mode enable/disable flag.

Comments

Used to control "monitor mode" in analog input functions. Enabling monitor mode causes analog input samples to looped back to analog output, with a one-sample delay, both before data acquisition is started, and during. If stimulus & response operation is in effect, input loopback automatically stops when stimulus output begins.

See Also

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_NUMCHAN

Description

Number of channels in analog I/O function.

See Also

DSP_CHANLIST

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_OFFSETIN

Description

Analog input data digital offset.

Comments

Specified in A/D samples. Value can be positive or negative and is added to analog input samples after digital scaling is applied (see DSP_SCALEIN).

See Also

DSP_SCALEIN

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_OFFSETOUT

Description

Analog output data digital offset.

Comments

Specified in D/A samples. Value can be positive or negative and is added to analog output samples after digital scaling is applied (see DSP_SCALEOUT).

See Also

DSP_SCALEOUT

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_OPMODE

Description

Operating mode.

Comments

Specifies processing or analog I/O function operating mode to Hypersignal DSP Source Code Interface.

See Also

DSP_BOARDCLASS

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP_OVERFLOW

Description

Overflow flag.

Comments

Indicates to host when overflow has occurred in processing or instrumentation function. Active only for DSP/analog hardware with fixed-point DSP devices.

See Also

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_PHZREQ

Description

Phase data calculation request flag.

Comments

Used in spectrum analyzer function.

See Also

DSP_LOGFLG1

DSP_LOGFLG2

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_PWRCOEFFA

Description

Coefficient "a" for power spectra calculation using exponential filter method.

Comments

Used in spectrum analyzer instrument function. Exponential filter is single-pole lowpass filter of form y[n] = a∗x[n] + b∗y[n–1].

See Also

DSP_PWRCOEFFB

DSP_PWRFLG1

DSP_PWRFLG2

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_PWRCOEFFB

Description

Coefficient "b" for power spectra calculation using exponential filter method.

Comments

Used in spectrum analyzer instrument function. Exponential filter is single-pole lowpass filter of form y[n] = a∗x[n] + b∗y[n–1].

See Also

DSP_PWRCOEFFA

DSP_PWRFLG1

DSP_PWRFLG2

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_PWRFLG1

Description

Power spectra calculation request flag for trace 1.

Comments

Used in spectrum analyzer instrument function.

See Also

DSP_PWRFLG2

DSP_PWRCOEFFA

DSP_PWRCOEFFB

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_PWRFLG2

Description

Power spectra calculation request flag for trace 2.

Comments

Used in spectrum analyzer instrument function.

See Also

DSP_PWRFLG1

DSP_PWRCOEFFA

DSP_PWRCOEFFB

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_RIDATAADDR

Description

Frequency domain or wavelet domain complex (real/imaginary) data base address.

Comments

For DSP/analog hardware with linear memory, real and imaginary values alternate locations. For hardware with vector memory, real values are in X: memory and imaginary values in Y: memory.

See Also

DSP_MAGDATAADDR

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_RIFLG

Description

Real/imaginary data flag.

Comments

Used to indicate that DSP/math function should also format and prepare real/imaginary data for host transfer.

See Also

DSP_RIDATAADDR

DSP_MAGDATAADDR

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP_SCALEIN

Description

Analog input digital scale factor.

Comments

An integer value specified in "Q-10" notation, to allow both gain and attenuation. Typical effective scaling range is from 1/1024 to 256 is achieved by multiplying desired value by 1024. Applied before digital offset value is added (see DSP_OFFSETIN).

See Also

DSP_OFFSETIN

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_SCALEOUT

Description

Analog output data digital scaling factor.

Comments

An integer value specified in "Q-10" notation, to allow both gain and attenuation. Typical effective scaling range is from 1/1024 to 256 is achieved by multiplying desired value by 1024. Applied before digital offset value is added (see DSP_OFFSETOUT).

See Also

DSP_OFFSETOUT

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_SERIALCTRL

Description

Control word for DSP onchip serial port configuration.

Comments

DSP/analog hardware types which use onchip serial ports to interface to external A/D or D/A converters most often require a fixed serial port control word value. However, some hardware types, most notably DSP32C and DSP3210, may allow some user-specified options in this value. In these cases, this value is active.

See Also

DSP_CODECCTRL1

DSP_CODECCTRL2

DSP_FSMODE

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_STMBUFLEN

Description

Stimulus data buffer length.

Comments

Stimulus data is output using dual-buffer switching mechanism; thus, total stimulus length is twice value of DSP_STMBUFLEN.

See Also

DSP_STMDATAADDR

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_STMDATAADDR

Description

Stimulus data base address in DSP memory.

Comments

For TMS320C2x and TMS320C5x DSP/analog hardware, this address is in program memory. For all other hardware types, this address is in data memory.

See Also

DSP_STMBUFLEN

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_TIMDATAADDR

Description

Time domain data base address in DSP memory.

Comments

Used for both file-based acceleration processing and analog I/O functions.

See Also

DSP_WINDATAADDR

DSP_RIDATAADDR

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_TRIGCHANLIST

Description

Analog input trigger channel list.

Comments

Each trace occupies a 4-bit channel field in this value, starting with trace 0 in bits 0..3.. For DSP/analog hardware types with 32-bit

floating-point DSP devices, this normally means a maximum of 8 channels can be specified.

See Also

DSP_TRIGLEVEL

DSP_CHANLIST

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_TRIGLEVEL

Description

Analog input trigger level.

Comments

Specified in A/D samples; can be either positive or negative. A value of zero indicates "freerun" trigger mode.

See Also

DSP_TRIGCHANLIST

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_WINSCL

Description

Scaling factor compensating for specified FFT or wavelet transform window type, if any.

Comments

Used by spectrum analyzer function when calculating correct linear magnitude scale factors.

See Also

DSP_WINDATAADDR

DSP_LOGFLG1

DSP_LOGCOEFFA

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_WINDATAADDR

Description

Time domain window base address in DSP memory.

Comments

Used for FFT or other DSP processing function, and spectrum analyzer instrument function.

See Also

DSP_WINSCL

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_XFERFLG1

Description

Transfer function calculation request flag in spectrum analyzer function for trace 1.

See Also

DSP_XFERFLG2

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode

DSP_XFERFLG2

Description

Transfer function calculation request flag for trace 2 in spectrum analyzer instrument function.

See Also

DSP_XFERFLG1

DSGetHVarMem

DSPutHVarMem

Related Users Guide Topics

DSP Source Code Interfaces for Hypersignal

DSP Source Code Interfaces for Hypersignal in Engine Mode